A First Digitally-Controlled Oscillator in a Deep-Submicron CMOS Process for Multi-GHz Wireless Applications

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Abstract—**A novel digitally-controlled oscillator (DCO) architecture for multi-GHz RF applications is proposed and demonstrated. It deliberately avoids any use of an analog tuning voltage control line. Fine frequency resolution is achieved through high-speed dithering. This enables to employ fully-digital frequency synthesizers in the most advanced deep-submicron digital CMOS processes which allow almost no analog extensions. It promotes cost-effective integration with the digital back-end onto a single silicon die. The demonstrator test chip has been fabricated in a digital 0.13 μm CMOS process together with a DSP. The DCO core consumes 2.3 mA from a 1.5 V supply and has a very large tuning range of 500 MHz. The phase noise is -112 dBc/Hz at 500 kHz offset.**

I. Introduction

Traditional designs of commercial frequency synthesizers for multi-GHz mobile RF wireless applications have almost exclusively employed the use of a charge-pump *phase-locked loop* (PLL), which acts as a *local oscillator* (LO) for both a transmitter and a receiver. Unfortunately, the design flow and circuits techniques required are quite analog intensive and utilize process technologies that are incompatible with a digital baseband, which nowadays is built in a low-voltage deep-submicron digital CMOS process with almost no analog extensions and very limited voltage headroom.

The aggressive cost and power reduction of a mobile wireless solution can only be realistically achieved by the highest level of integration, and this favors digitally-intensive approach. A digitally-controlled oscillator which deliberately avoids any analog tuning voltage controls is presented in this paper. This allows for its loop control circuitry to be implemented in a fully digital manner.

II. Varactor in a Deep-Submicron CMOS

Frequency tuning of a low-voltage deep-submicron CMOS oscillator is quite a challenging task due to its highly nonlinear frequency-vs.-voltage characteristics and low voltage headroom. Fig. 1 (top) shows normalized representative curves of a MOS varactor capacitance vs. control voltage (C-V curve) for both a traditional CMOS process and a deep-submicron process. Previously, a large linear range of the C-V curve could be exploited for a precise

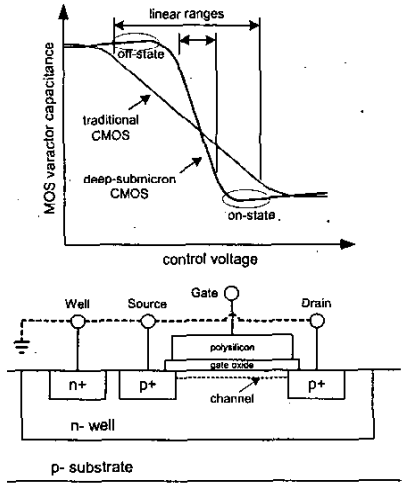

Fig. 1. Idealized capacitance vs. voltage curves of a MOS varactor (top), and a physical structure of a PMOS transistor used as a varactor when the source, drain and well tie-offs are tied to ground (bottom)

and wide operational control of frequency. With a deep-submicron process, the linear range now is very compressed and has undesirable high gain ($K_{VCO} = \Delta f/\Delta V$) which makes the oscillator extremely susceptible to noise and operating point shifts.

An example C-V curve of an actual PMOS varactor used in the proposed design for the acquisition mode is shown in Fig. 2. Because of the well isolation properties in this N-well process, the PMOS device (bottom of Fig. 1) is a better candidate for a varactor. The device has the following channel length and width dimensions and finger multiplicity: L=0.5 μm, W=0.6 μm, N=8 fingers x 12 x 2. The data was measured and de-embedded from a test structure at the intended frequency of operation of 2.4 GHz.

The slight drop of capacitance in the "flat" strong inversion region in Fig. 2 had not been of any practical significance until the advent of deep-submicron CMOS

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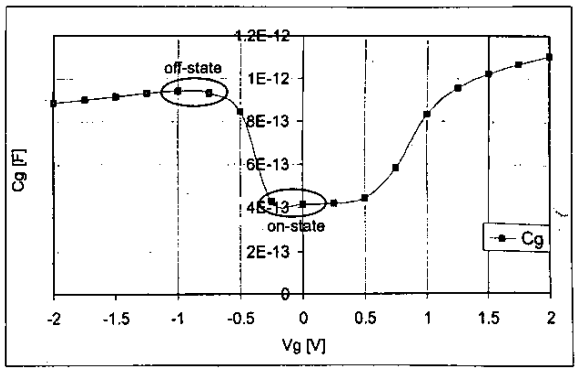

Fig. 2. Gate capacitance vs. gate voltage of a measured PMOS varactor

processes. It is due to the depletion layer being created in the gate polysilicon [1] which is less doped and much thinner than in the past.

It was experimentally confirmed that in this process the PPOLY/NWELL inversion-type varactor features more distinctly defined operational regions than does the accumulation-type varactor. In fact, the flat on-state region of the depletion mode and the flat off-state region of the inversion mode (Fig. 2) are used as two stable binary-controlled operating points.

III. Fully Digital Control of Oscillating Frequency

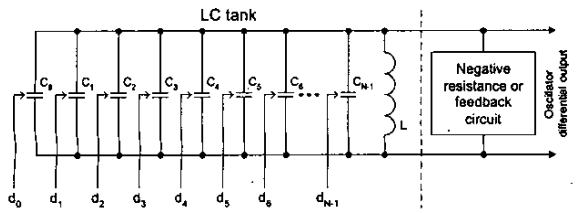

Fig. 3. LC-tank-based oscillator with switchable capacitors

The proposed solution to control the oscillating frequency could generally be summarized as follows: A method of weighted binary switchable capacitance devices, such as varactors, is proposed. An array of varactors (Fig. 3) could be switched into a high-capacitance mode or a low-capacitance mode individually by a two-level digital control voltage bus, thus giving a very coarse step control for the more-significant bits, and less coarse step control for the less-significant bits. In order to achieve a very fine frequency resolution, the LSB bit could possibly be operated in an analog fashion. (A similar idea is used in [2] which employs a hybrid of digital oscillator control for PVT and *analog* control for acquisition and tracking.) However, this requires a DAC and does not fundamentally solve the problem of the nonlinear VCO gain (K_{VCO}) characteristics. A better solution is to dither the LSB digital control bit (or multiple bits), thus controlling its time-averaged value with a finer resolution. Consequently, each varactor could be allowed to stay in only one of the two regions where the capacitance sensitivity is the lowest and the capacitance difference between them is the highest. These two operating regions are shown by the ovals in Fig. 2.

It should be noted here that so far there have not been any reports in the literature on the *fully* digital control of oscillators for RF applications. Lack of the fully digital control is a severe impediment for the total integration in a deep-submicron CMOS process. Due to the fact that there are several disclosures on the ring-oscillator-based DCO's for clock recovery and clock generation applications, where the frequency resolution and spurious tone level are quite relaxed, it seems that the latter two concerns have been an effective deterrent against digital RF synthesizers for wireless communications. Fortunately, the simultaneous solution to both these problems lies in a high-rate dithering of the LSB varactors.

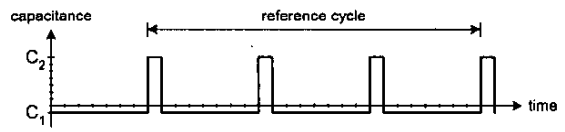

Fig. 4. DCO dithering by changing the discrete capacitance at high rate

The proposed idea of high-rate dithering of LSB capacitors is illustrated in Fig. 4. It is similar in principle to the fractional-N division ratio dithering. Instead of applying a constant input that would select capacitance C_1 or C_2, where $C_2 = C_1 + \Delta C$ with ΔC being an LSB capacitor, during the entire reference cycle, the selection alternates between C_1 and C_2 several times during the cycle. In the example, C_2 is chosen one-eighth of the time and C_1 is chosen the remaining seven-eighths. The average capacitance value, therefore, will be one-eighth of the $C_2 - C_1$ distance over C_1. It should also be noted that the resolution of the time-averaged value relies on the dithering speed. Without any feedback that would result in a supercycle, the dithering rate has to be higher than the reference cycle rate times the integer value of the resolution inverse (eight in this case). Therefore, there is a proportional relationship between the frequency resolution improvement and the dithering rate.

The dithering pattern shown in Fig. 4 is not random at all and is likely to create spurious tones. It is equivalent to the first order $\Sigma\Delta$ modulation [3]. If the LSB varactor has a frequency resolution of Δf and is dithered at a rate of f_m then it will produce two spurs f_m away on both sides of the oscillating frequency with the power level of $20\log(\beta/2)$

relative to the carrier, where $\beta = \frac{4}{\pi}\frac{\Delta f}{f_m}$. For example, if the step size of the LSB varactors is Δf = 23 kHz and the dithering clock is 600 MHz such that f_m = 300 MHz, then the generated spur level is only -92 dBc.

A second and third order of ΣΔ randomization is used in order to effectively eliminate the already-low spurious content.

IV. Oscillator Core

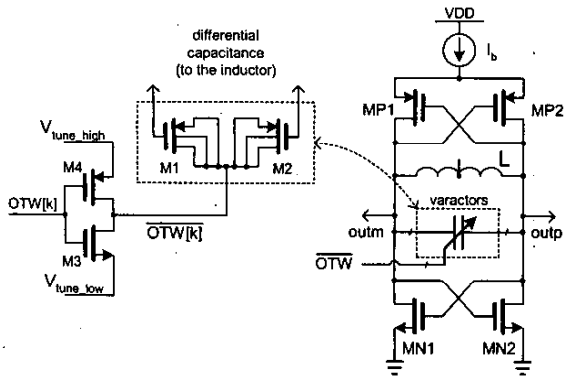

Fig. 5. Differential varactor and an inverting driver (left); ideal schematic of the DCO oscillator core (right)

Fig. 5 (left) shows an implementation of the differential varactor and the preceding driver stage. The V_{tune_high} and V_{tune_low} rail supply levels of the inverter are set to correspond with the two stable operating points, off-state and on-state of the *oscillator tuning word* (OTW), respectively, as shown in Fig. 2. The varactor used in this work is a differential configuration built upon the basic structure described in conjunction with Fig. 1 and Fig. 2. The balanced capacitance is between the gates of both PMOS transistors M1 and M2, whose source, drain and backgate connections are shorted together and tied to the M3/M4 inverter output. Because of the differential configuration, only one-half of the single PMOS capacitance is achieved, which enhances frequency resolution.

Ideal schematic of the DCO oscillator is shown on the right of Fig. 5. It is similar to [4], except for the exclusive use of digitally-controlled varactor array.

V. DCO Architecture

Fig. 6 illustrates the proposed idea to increase frequency resolution of the DCO. The fractional part employs a time-averaged dithering mechanism to further increase the frequency resolution from the basic of 23 kHz. The dithering is performed by a digital ΣΔ modulator (SDM) that produces a high-rate integer stream whose average value equals the lower-rate fractional input. The digital SDM is considered an essential part of the proposed DCO solution for wireless applications.

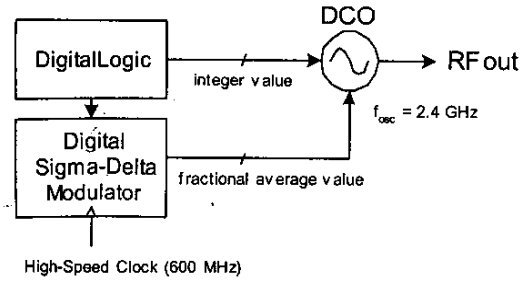

Fig. 6. Improving frequency resolution with ΣΔ dither of DCO varactors

The ΣΔ modulator is built as a third-order MESH-type structure [5] that could be efficiently scaled down to a lower order. It is clocked by the 600 MHz clock.

As explained earlier, the dithering method trades the sampling rate for the granularity. As an example of the implemented design, if the frequency resolution of the 2.4 GHz DCO is Δf^T = 23 kHz with a 13 MHz update rate, then the effective time-averaged frequency resolution, within one reference cycle, after the 600 MHz ΣΔ dither with five sub-LSB bits would be $\Delta f^{T-\Sigma\Delta}$ = 23 kHz / 2^5 = 718 Hz. The frequency resolution improvement achieved here is 2^5 = 32. This roughly corresponds to the sampling rate speedup of 600 MHz / 13 MHz = 26.

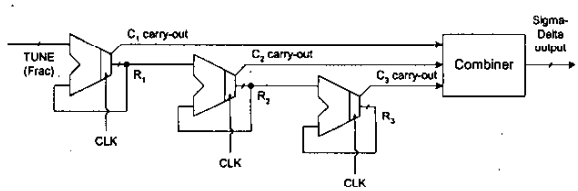

Fig. 7. MESH-3 ΣΔ digital modulator structure

The structure of the digital ΣΔ modulator is depicted in Fig. 7. It is implemented as a 3-rd order MESH-type architecture. Its topology is based on [3]. The original structure is not the best choice for high-speed designs because the critical path spans through all the three accumulator stages and the carry sum adders. A critical path retiming transformation needed to be performed in order to shorten the longest timing path to only one accumulator so that the 600 MHz clock operation could be reached. The combiner circuit merges the three single-bit carry-out streams such that the resulting multi-bit output satisfies the 3-rd order ΣΔ spectral property. The ΣΔ stream equation below is a result of register retiming of the architecture originally described in [3].

$$out_{\Sigma\Delta} = C_1 \cdot D^3 + C_2 \cdot (D^2 - D^3) + C_3 \cdot (D - 2D^2 + D^3) \quad (1)$$

where $D \equiv z^{-1}$ is the delay element operation.

VI. Implementation and Results

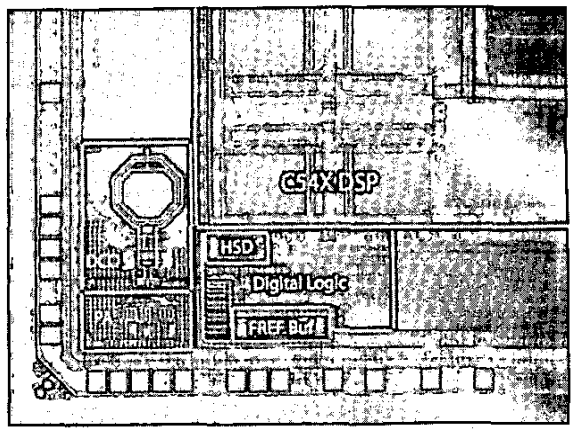

Fig. 8. Chip micrograph of the RF area.

Fig. 8 is a die micrograph of the RF frequency synthesizer area. It is located in the lower-left corner and occcupies 0.54 mm^2. The inductor itself occupies a 270 μm x 270 μm square. High-speed Digital (HSD) running at 600 MHz performs the $\Sigma\Delta$ dithering of the DCO varactors. The companion C54X DSP digital baseband occupies 6 mm^2. This area comparison clearly illustrates the benefits of RF integration into digital.

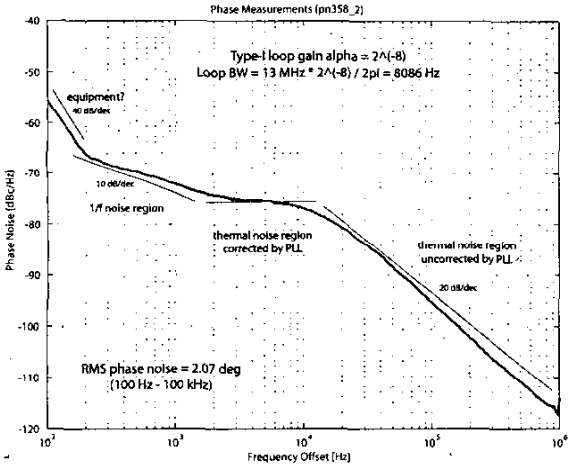

Fig. 9. Measured synthesizer phase noise with the presented DCO: wide loop bandwidth of 8 kHz

Measured phase noise of an all-digital frequency synthesizer with the presented DCO is shown in Fig. 9. The phase noise is -112 dBc/Hz at 500 kHz offset and is actually constrained by operating in the current limited region. Fig. 10 reveals the spurious tones emited during the locked operation in the wide span of 1.5 GHz. The close-in spurs lie below -60 dBc and are due to FREF coupling through substrate and power/ground lines. The far-out spurs are vanishingly small and well below the floor of -80 dBc. The carrier power level is at -1 dBm. The DCO core consumes 2.3 mA from a 1.5 V supply and has a very large tuning range of 500 MHz.

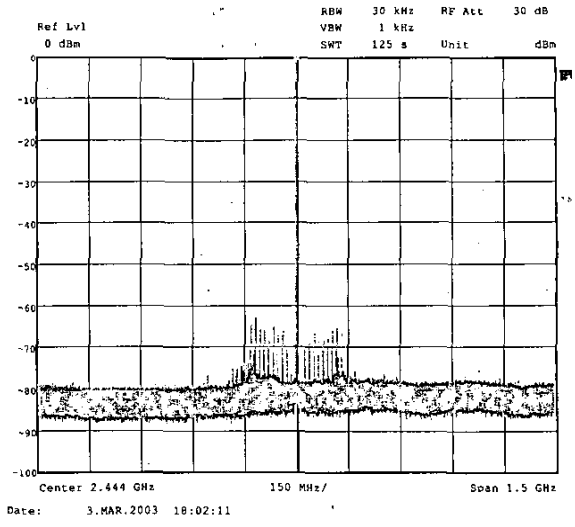

Fig. 10. Spurious tones generated by a synthesizer with the presented DCO using $\Sigma\Delta$ varactor randomization

VII. Conclusion

A novel *digitally-controlled oscillator* (DCO) architecture for multi-GHz RF applications has been proposed and demonstrated in this paper. This enables to employ fully-digital frequency synthesizers in the most advanced deep-submicron CMOS processes with almost no analog extensions. It allows cost-effective integration with the digital back-end onto a single silicon die. A 2.4 GHz DCO and its peripheral circuitry have been fabricated in a digital 0.13 μm CMOS process and integrated with a DSP. It demonstrates feasibility of the digitally-controlled oscillator for RF multi-GHz applications.

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